IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HOON KIM

Serial No.:	10/798,574	Examiner:	FLYNN, NATHAN J.
Filed:	12 March 2004	Art Unit:	2826
For:	THIN FILM TRANSISTOR AND METHOD FOR FABRICATING THE SAME		

PETITION UNDER 37 C.F.R. §1.102

Mail Stop: OFFICE OF SPECIAL PROGRAMS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant respectfully petitions the Commissioner to designate the above-referenced application as "Special" in accordance with the *Manual of Patent Examining Procedure* (MPEP) §708.02 (VIII), (8th Ed., Revision 2, May 2004), and as reason therefore states that:

Folio: P57012
Date: 11/1/04
I.D.: REB/sb

STATEMENT OF FACTS

1. The present application is assigned by the Applicant to Samsung SDI Co., Ltd. in an instrument that was recorded in the U.S. Patent & Trademark Office on Reel 015079, at Frame 0790 on the 12th day of March 2004, having the principal place of business at 575, Shin-Dong, Yeongtong-Gu, Suwon-si, Gyeonggi-do, Republic of Korea, a manufacturer of sufficient presently available capital and facilities, has long established relations with vendors and contract to manufacture the present invention in quantity if a patent is granted on the present application.

2. The Applicant has worked to develop and design prototypes of several constituent components for embodiments of the invention claimed; over the past three (3) years. Samsung SDI Co., Ltd. has spent about in excess of $1,000,000.00 for wages, facilities, parts and materials, insurance and taxes, to research the invention claimed and to design, develop and build prototypes of the several constituent elements useful in the practice of the invention as claimed.

3. All pending claims are directed to a single invention.

4. Pursuant to §708.02 (VIII)(B) of the *MPEP* (Rev. 2, May 2004), if the Office determines that all the claims presented are not obviously directed to a single invention, Applicant will make an election in response to the established telephone restriction practice.

5. In accordance with §708.02 (VIII)(C) of the *MPEP* (Rev. 2, May 2004), and 37 C.F.R.

§1.102, Applicant has made a careful and thorough search of the prior art, and presents in the *Statement* filed simultaneously with this *Petition*, an analysis of the pending claims in the light of the art listed and discussed in the accompanying *Information Disclosure Statement* that is also filed simultaneously with this *Petition*.

6. In accordance with §708.02 (VIII)(D) of the *MPEP* (Rev. 2, May 2004), and 37 C.F.R. §1.102, Applicant submits with the accompanying *Statement* one copy of each of the references deemed most closely related to the subject matter encompassed by the pending claims.

7. In accordance with §708.02 (VIII)(E) of the *MPEP* (Rev. 2, May 2004), and 37 C.F.R. §1.102, Applicant submits with the accompanying *Statement* a detailed discussion of the references, which discussion points out, with the particularity required by 37 CFR §1.111(b) and (c), how the claimed subject matter is patentable over the references.

REMARKS

Pursuant to 37 C.F.R. § 1.102, explained in §708.02 of the *Manual of Patent Examining Procedure*, 8th Ed., Rev. 2, May 2004, Applicant is entitled to have this application made special, as a new application by demonstrating compliance with §708.02 (VIII) of the Manual.

As explained in the accompanying Statement, Samsung SDI Co., Ltd. requests the Office to advance the prosecution and examination of their above-captioned U.S. patent application, without further delay in the U.S. PTO process, in view of the Applicant's and Samsung SDI Co., Ltd.'s compliance with §708.02 (VIII)(A) through (E) of the *MPEP* (Rev. 2, May 2004), and 37 C.F.R. §1.102, as demonstrated by the accompanying *Statement* and *Information Disclosure Statement.*

A fee of $130.00 is incurred by 37 C.F.R. § 1.17(h). Applicant's check drawn to the order of Commissioner accompanies this Petition. Should the check become lost, be deficient in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

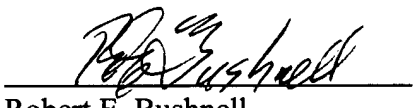
RELIEF REQUESTED

The Commissioner is therefore, respectfully requested to:

A. Grant this *Petition*, designate the application as "Special", and accelerate the examination of the application;

B. Grant such other and further relief as justice may require.

Respectfully Submitted



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STATEMENT UNDER 37 C.F.R. §1.102

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Sir:

In accordance with 37 C.F.R. §1.102 and the procedure set forth in the *Manual of Patent Examining Procedure* (MPEP) §708.02 (VIII), (8th Ed., Rev. 2, May 2004), Petitioner submits this statement in support of the accompanying *Petition* under 37 C.F.R. §1.102 and the accompanying *Information Disclosure Statement.*

Folio: P57012
Date: 11/1/04
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REMARKS

Status of the Claims

Claims 1 through 20 are pending in this application. No claims are amended. Claims 1, 7, 13 and 17 are independent claims.

The following is a detailed discussion of the references, which discussion points out, with particularity required by 37CFR§1.111(b) and (c), how the claimed subject matter is patentable over the reference. MPEP §708.02 (VIII, Special Examining Procedure For Certain New Applications-Accelerated Examination).

Pre-Examination Search

A pre-examination search was made through Class 257, subclasses 021, 066, 072, 103, 314, 330, 339, 347, 401; class 349, subclass 043; class 438, subclasses 149, 163, 270, 297, 303; and class 999, subclasses 023.700, 038, 101, the Japanese laid-open patent collection, and the Republic of Korea laid-open patent collection.

Detailed Discussion of The References

1.U.S. 6,777,747 Yedinak, Class 257, Subclass 339

Concerning claims 1, 7, 13, and 17, Yedinak fails to disclose a thin film transistor as claimed in claim 1 as there is no disclosure of a thin film. Yedinak instead concerns an insulated gate bipolar transistor used for example in power systems and control devices of automobiles.

Yedinak fails to disclose said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer as claimed in claim 1 of the present inveniton as seen by the flat buffer regions without a step shown in figures 3A and 3B of Yedinak.

Yedinak fails to disclose said step being a half or less of the thickness sum of said activation layer and gate insulation layer as claimed in claim 1 because Yedinak fails to disclose a step formed between a lower part and activation layer as shown in figures 3A and 3B of Yedinak.

Moreover, since Yedinak fails to disclose a step in the buffer layer, Yedinak also fails to disclose said buffer layer has a step to such a degree that thickness of said gate insulation layer is not changed on said side wall of said buffer layer as claimed in claim 2 of the present invention.

Concerning claim 3, Yedinak discloses the buffer thickness and other measurements in col.

5, lines 15-24, but there is no disclosure of a thickness of the gate insulation layer is at least 400 Å when the thickness of SPC polysilicon is 300 Å and step is 350 Å in the activation layer as claimed by the present invention. The same is true for claims 4-6 as the gate insulation layer measurement is not disclosed as related to a polysilicon and step.

Concerning claim 7, Yedinak fails to disclose depositing an amorphous silicon layer on a substrate equipped with buffer layer. An amorphous silicon is never mentioned by Yedinak.

Yedinak also does not disclose forming a polycrystalline silicon layer by crystallizing said amorphous silicon layer and forming an activation layer by etching said polycrystalline silicon layer according to claim 7 of the present invention. In col. 1, lines 15-30, Yedinak states, "A gate conductive layer, typically polysilicon 19, covers the insulating layer 17 and forms a gate electrode. Another insulating layer 21 covers the polysilicon and a metal contact layer 23 contacts the source 2 and the base 3 of each cell. The above description is for a planar device with the gate on the surface. However, the IGBT may be fabricated with a trench gate. See FIG. 3b." However, no such formation of polycystalline silicon layer or activation layer.

Moreover, Yedinak fails to disclose with etching time being controlled in said activation layer forming process and activation layer surface treatment process so that step between a lower part of gate in the buffer layer and a part except the lower part of said gate has a step value corresponding to a half or less of the thickness sum of said activation layer and gate insulation layer according to claims 7 and 17 of the present invention since there is no step between a lower part of gate in the buffer layer as seen in figures 3A and 3B of Yedinak.

2. U.S. 6,534,788 Yeo et al. Class 257, Subclass 072

Concerning claims 1 and 13, Yeo et al. fails to disclose said step of the buffer layer being a half or less of the thickness sum of said activation layer and gate insulation layer. As seen in figure 2 of Yeo, a buffer layer 23 is included between an active layer 24 and the lower gate electrode 21G and a gate insulation layer is between the gate electrode 26G and the gate insulation layer 25 between the gate electrode 26G and the active layer 24. However, there is no disclosure as to the relationship of the thicknesses of the buffer layer with the activation layer and the gate insulation layer.

Moreover, concerning claims 7 and 17, Yeo et al. also fails to disclose etching time being controlled in said activation layer forming process and activation layer surface treatment process to accommodate a step between a lower part of gate in the buffer layer and a part except the lower part of said gate has a step value corresponding to a half or less of the thickness sum of said activation layer and gate insulation layer because Yeo et al fails to disclose the relationship of buffer thickness, especially the step region of the buffer as related to the activation layer and the gate insulation layer.

In addition concerning claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Yeo fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer. There is quantification of the thicknesses made in Yeo. The buffer layer, for example, is disclosed as covering an exposed surface of the substrate including the source and

drain electrodes as seen in col. 13, lines 12-13 of Yeo.

3. US6,528,855 Ye et al. Class 257, Subclass 401

Ye et al., concerning claims 7 and 17, fails to disclose forming an activation layer by etching said polycrystalline silicon layer since the gate area is defined by etching crystal silicon and not etching polycrystalline silicon as mentioned specifically in the col. 3, lines 1-2 of Ye.

Concerning claims 1, 13 and also claims 7 and 17, Ye fails to disclose step in the buffer being a half or less of the thickness sum of said activation layer and gate insulation layer because for example figure 1A, which is the cross-sectional view of the MOSFET structure of Ye, shows no such relationship in Ye.

4. US6,509,234 01/03 Krivokapic Class 438, Subclass 270

Concerning claims 1, 7, 13 and 17, Krivokapic fails to teach or suggest a buffer layer as claimed in the present invention including for example the buffer including a step and the step in the buffer being a half or less of the thickness sum of said activation layer and gate insulation layer. In col. 5, lines 21-33 of Krivokapic states, "When a high-K material is selected as the gate dielectric 34, a buffer interface (not shown) can be used between the layer of semiconductor material 16 and the gate dielectric 34. The buffer interface can be, for example, an oxide layer having a thickness of about 0.5 nm to about 0.7 nm. The buffer interface acts to reduce diffusion and/or penetration of atoms from the high-K dielectric material into the layer of semiconductor material 16 that could lead to a degradation in channel mobility. In addition, the buffer interface may act to retard reaction of the high-K material with the layer of semiconductor material 16. In one embodiment, the buffer interface can be formed from the same layer of material used to form the oxide layer 38." In col. 12, lines 39-40 the body is mentioned to be 50 angstroms. Instead of the relationship of the step of the buffer to the activation and gate insulation layer claimed in the present invention, Krivokapic teaches "etching the layer of semiconductor material to form a recess therein, the recess formed in at least the body region of the layer of semiconductor material such that a thickness of the body is less than a thickness of the source and the drain" as seen in col. 12, lines 21-26 of Krivakapic.

5. US 6,396,079 Hayashi et al. Class 257, subclass 066

Concerning claims 1, 7, 13 and 17, Hayashi fails to teach or suggest a buffer layer including a step and especially there is no mention of the step being half or less of the thickness sum of the activation layer and the gate insulation layer. In figures 1, 2 and 3 of Hayashi includes a flat buffer layer 2 located between the glass substrate 1 and the gate insulating film 5 and gate electrode G.

6. US 6,033,941 Yang Class 438, Subclass 163

With regard to claims 1, 7, 13 and 17, Yang fails to disclose, teach or suggest a buffer layer including a step and especially there is no mention of the step being half or less of the thickness sum of the activation layer and the gate insulation layer because Yang teaches instead of a buffer oxide or buffer nitride layer 15 between the gate oxide layer 16 and the offset region 14b of the polysilicon body layer 14, where the buffer layer 15 includes no step as seen in figure 2 of Yang, which is the section view of the thin film transistor of Yang having an asymmetric arrangement of the gate electrode 17 and the offset region 14b.

Concerning claims claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Yang fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer. There is no quantification of the thicknesses made in Yang. In stead Yang only discloses that "silicon substrate, to have a predetermined thickness. A trench having a predetermined thickness" col. 3, lines 20-26, but no teachings of specific thicknesses.

7. US5,510,640 Shindo Class 257, Subclass 347

With regard to claims 1, 7, 13 and 17, Shindo fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. No such comparision is taught by Shindo. Shindo on figure 4E (first embodiment) and 5C (second embodiment) discloses a lower barrier layer 12 with a step formed on the substrate 11 and also includes gate electrode 17 and the interlayer insulating film 18 in figure 4E and WSi layer 27 in figure 5C. The gate electrode 17 has a polysilicon 17' with a thickness of 500 Angstroms (figure 5C). Shindo also discloses the silicon oxide barrier layer 12' being 3700 Angstroms. Col. 5, lines 19 through col. 6, line 55. However, the step in the barrier layer 12 is never compared to the activation and gate insulation layer. Shindo instead discloses "The thickness of said channel region is smaller than the thickness of said source drain region". col. 8, lines 17-18.

Concerning claims claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Shindo fails to disclose the range of thickness of the gate insulation layer and the thickness of the step in the activation layer as shown above mentions the polysilicon being 500 Angstroms only and the barrier layer being 3700 Angstroms.

8. US5,196,717 Hiroki et al. Class 257, Subclass 021

With regard to claims 1, 7, 13 and 17, Hiroki fails to disclose, teach or suggest a buffer layer including a step and especially there is no mention of the step being half or less of the thickness sum of the activation layer and the gate insulation layer because the buffer layer 15 of the photoelectric field effect transistor shown in figure 2A and buffer layer 25 in figure 3A include no step portion.

9. US5,173,753 Wu Class 999, Subclass 023.700

With regard to claims 1, 7, 13 and 17, Wu fails to disclose, teach or suggest a step of the

buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. The gate was given to be a thickness of 2,000 Angstroms, the gate insulating layer 6 between 200 nm to 300 nm and the active layer from 100 nm to 300 nm and the passivation layer 10 is close to 300nm (figure 5 and col. 3, lines 51 through col. 4, lines 2), but no comparision with a step of the buffer layer.

10. US5,144,401 Ogura et al. Class 999, Subclass 038

With regard to claims 1, 7, 13 and 17, Shindo fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer.

As seen in figure 18A, the buffer layer has a "T" shape. col. 11, lines 48-58. However, there is no comparison of the thickness of the activation layer and gate insulation layer with the step of the buffer layer as claimed in the present invention. The only reference to thickness is the reduction of the thickness of the first base layer (col. 9, lines 1-6) and the buffer being 10 micrometers or larger. col. 9, line 1.

In addition concerning claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Ogura fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer. Ogura, the only quantified thickness mentioned was the following, "The MOS thyristor of FIG. 12, the averaged impurity concentration of n+ type buffer 30 is, for example, $2x10^{16}/cm^3$ or more, and the thickness is 10 micrometers or larger." col. 8, line 65 through col. 9, line 6.

11. US4,715,930 Diem Class 999, Subclass 101

With regard to claims 1, 7, 13 and 17, Diem fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. Diem only discloses a hydrogenated amorphous silicon layer 8 deposited on the insulating layer 6, with the remaining silicon layer and "This final partial etching operation acts in the same way on the displacement 11 and step 9a (FIG. 6) and leads to the appearance of a second step 11a, which is added to the first step 9b on the edges of the remaining silicon layer 8c".

12. US4,287,661 Stoffel Class 438, Subclass 303

With regard to claims 1, 7, 13 and 17, Stoffel fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. Stoffel discloses a polysilicon conductor including a first and second polycrystalline silicon layer 40 and 30, respectively, on a monocrystalline silicon 22 as shown in figures 7 and 8. The thickness of the polycrystalline silicon after etching is between 200 and 1000 Angstroms. col. 6, lines 45-53. The conductor also includes a silicon dioxide layer 38 and 42. The thickness of the recessed oxide regions is of the order of 9000 to 12,000 Angstroms. co. 3, lines 10-16. The layer of the

polysilicon deposited on the insulator is also coated with the thickness of the gate dielectric. Therefore, no relationship of the step in the buffer layer with an activation layer and gate insulation layer is made and additionally concerning claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Stoffel fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer as claimed according to the thicknesses disclosed above.

13. US4,035,198 Dennard et al. Class 438, Subclass 297

With regard to claims 1, 7, 13 and 17, Dennard fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. Dennard includes a field effect transistor that has gate insulator 38, a dielectric insulation layer 60, a thick layer of oxide 64 as seen in figure 8 (8A-8I) and a field isolation layer 34. FET gate insulator is a layer of silicon dioxide about 200 to about 1000 A in thickness, gate electrode material being a polysilicon of 1500 A to 5000 A and thick layer of insulation is 2500 to 5000 A thick (col. 14, lines 43-45 and col. 15 , lines 19-23). Therefore, no relationship of the step in the buffer layer with an activation layer and gate insulation layer is made and additionally concerning claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Dennard fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer as claimed according to the thicknesses disclosed above.

14. US publication 2004-0173812 Currie et al. Class 257, Subclass 103

With regard to claims 1, 7, 13 and 17, Currie fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. Currie et al. discloses a "T" shaped cross section of the trench structure 55 which can be a dielectric such as silicon dioxide or an amorphous semiconductor such as amorphous silicon. On the substrate is the graded buffer layer 14 and pad oxide portions 26a and 26b(Fig. 8) a gate 110 with a gate dielectric 114 (Figs. 10A-10C). According to Currie, "The active device area bounded by trench structures 55a-55d parallel to the current flow and perpendicular to the gate. Referring to FIG. 10a, the active area length is along the 10c-10c line." paragraph 70 of Currie.

However, there is no relationship of the step in the buffer layer with an activation layer and gate insulation layer being made. Currie discloses of the thicknesses of the strained layer 18 of being 50-1000 A (paragraph 33 of Currie) and the insulation layer 28 of being 200-300 A (paragraph 41 of Currie), but the thickness of the gate insulation, activation layer and the buffer layer of the present invention is not clearly disclosed and therefore, the comparison of the step of the buffer with the other layers cannot be taught or suggested by Currie.

15. US publication 2004-0084722 Yamaguchi et al. Class 257, Subclass 330

Yamaguchi fails to disclose with said buffer layer having a step formed between a lower part

of said activation layer and a part except said lower part of said activation layer as claimed in claims 1, 7, 13 and 17. Yamaguchi include p buffer layers 9 adjacent to trenches 4 with gate electrode 6 surrounded by gate insulating film 5. However, as seen in figure 1, Yamaguchi fails to disclose a buffer having a step and the buffer being formed between the lower part of the activation layer and the part except the lower part of the activation layer. Yamaguchi's buffer layer 9 as seen in figure 1 is a flat structure without a step located as claimed in the present invention. On the other hand, in figure 24, the p buffer layers 9 do include n layers 28, but the buffer layers 9 are below an insulating film 10 and above the n base layer 1, and therefore, Yamaguchi does not disclose buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer as claimed.

Moreover, concerning claims 1, 7, 13 and 17, Yamaguchi fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer since no thickness measurements and comparison was made in the specification.

In addition since no thickness measurements were quantified, the concerning claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Yamaguchi fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer as claimed.

16. US publication 2004-0005740 Lochtefeld et al. Class 438, Subclass 149

Yamaguchi fails to disclose with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer as claimed in claims 1, 7, 13 and 17. According to figure 8A, Lochtefeld includes a gate 212, gate dielectric 210, source and drain regions, while figure 15C discloses a process of forming the semiconductor device of Lochtefeld with a graded buffer layer 14 below the relaxed layer 16. However, as seen in figure 8A and 15C, there is no step in the buffer layer as claimed in the present invention.

Moreover, concerning claims 1, 7, 13 and 17, Yamaguchi fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer since as shown above, Yamaguchi fails to teach or suggest a step of the buffer as arranged in the claims 1, 7, 13, 17.

17. US publication 2003-0122178 Yang Class 257, Subclass 314

Yang '178 fails to disclose with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer where the step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer as claimed in claims 1, 7, 13 and 17. Yang '178 discloses a flash memory with a T-shaped floating gate that includes a buffered layer 30 as shown in figure 2E between a conductive layer 70 and oxide layer 20 on the semiconductor substrate 10 and formed with a trench 60 that goes through the buffered and oxide layers.

The buffered layer of Yang '178 is formed between 200 and 2500 A, while the conductive

layer is between 300 to 3000 A. (paragraph 14 of Yang '178). Therefore, concerning claims 1, 7, 13 and 17, Yamaguchi fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer since as shown above, Yamaguchi fails to teach or suggest a step of the buffer as arranged in the claims 1, 7, 13, 17 and with the respective comparison of the step portion.

18. US publication 2002-0054247 Hwang et al. Class 349, Subclass 043

With regard to claims 1, 7, 13 and 17, Hwang fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. Hwang discloses a gate electrode 122 formed on a substrate 110 and with a gate insulation layer 130, active layer 141 and the passivation layer 170 as shown in figure 3 and figure 4B also shows the amorphous silicon layers 140 and150 below the metal layer 160. The photoresist layer thickness was given as less than 3 microns, gate electrode between 2000 and 5000 A. (claims 2 and 5 of Hwang).

Concerning claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Hwang fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer as claimed according to the thicknesses disclosed above that only discloses the thicknesses of the photoresist layer and the gate electrode.

19. US patent 6,746,904 Van der Zaag et al. Class 438, Subclass 149

With regard to claims 1, 7, 13 and 17, Van der Zaag fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. Van der Zaag discloses on figure 5 electrodes 26 and 28 with gate electrode on insulating substrate 4 along with amorphous silicon layer 8 and insulating layer 6. Van der Zaag discloses the height of the upper surface of the gate electrode above the substrate is in the range of 0.05 to 1.5 microns (claim 8 of Van der Zaag). The insulating layer 6 may be a single layer of about 300 nm (col. 3, lines 58-65). The amorphous silicon layer 8 is of around 160nm and the contact layer 10 being 40 nm (col. 4, lines 1-6). Therefore, there is no disclosure or teaching or suggestion of the step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer.

Concerning claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, Hwang fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer as claimed according to the thicknesses disclosed above that only discloses the thicknesses of the photoresist layer and the gate electrode.

20. JP 63-093150 04/88 JAPAN (Minami et al. JP '150)

JP'150 fails to disclose with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer as claimed in claims

1, 7, 13 and 17.

JP'150 does include a polycrystalline silicon 12 on the gate electrode 6, a passivation film 11, a gate oxide film 5 as seen in figure 1a through 1f. As seen in figure 2a through 2d, the p type substrate 8 includes on the sides the field oxide film 9 and with a gate electrode 6 above the substrate 8. A doixide film 13 and a polycrystalline silicon 14 are also on the gate electrode 6. A flat gate oxide film 5 is on the substrate 8 and the source-drain regions 1 and 2. However, no step is seen in a buffer layer with a lower part of the activation layer as claimed in claims 1, 7, 13 and 17.

21. JP 61-078138 04/86 JAPAN (JP '138, Anraku, et al.)

With regard to claims 1, 7, 13 and 17, JP '138 fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. Looking at figure 1(g) of JP '138, on the substrate 1 are formed the field oxide film with the first and second gate oxide films 3 and 7, then on the field oxide film is the polycrystalline layer formed. Therefore, there is no disclose as to the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer, where the buffer layer having the step is formed between a lower part of said activation layer and a part except said lower part of said activation layer. The comparison is no disclosed.

22. JP 02-031464 02/90 JAPAN (JP '464, Kawarasaki et al.)

JP '464 fails to disclose a polycrytalline silicon layer as claimed in claims 17 and 7 and an amorphous silicon layer as claimed in claim 7. Looking at figure 1(f) of JP '464, an oxide film 4 is formed on the substrate 1, but then on the substrate 1 is also a single crystal silicon. The polycrystalline silicon 3 is not seen in the final product 1(f), but only in the interim product as seen in figure 1(a).

Concerning claims 1, 7, 13 and 17, JP '464 fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer. As seen in figure 1(f) a gate sheet dioxide film 7 is formed on the substrate 1 and depletion layers 12 are next to the source and drain regions 11. In figure 2(c), on the other hand, a gate dioxide region 9 is formed above the source and drain regions while there is no hexagonal shaped cross-section of the oxide film in the substrate 1 as seen in figure 1(g). Looking, therefore, at both figures 1(f) and 2(c) there is no disclosure of the buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer. Moreover, the step of a buffer layer is not taught or suggested to being half or less of the thickness sum of the activation layer and the gate insulation layer as claimed in claims 1, 7, 13 and 17 as no comparison is made.

23. JP 2004-153112 05/04 JAPAN (JP'112, Yamaguchi, et al.)

JP '112 is related to the US publication 2004-0084722 to Yamaguchi, et al., since JP 2004-153112 (application no.2002-318059) is the priority document for US publication 2004-

0084722 to Yamaguchi, et al.

JP '112 fails to disclose with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer as claimed in claims 1, 7, 13 and 17. JP '112 include p buffer layers 9 adjacent to trenches 4 with gate electrode 6 surrounded by gate insulating film 5. However, as seen in figure 1, JP '112 fails to disclose a buffer having a step and the buffer being formed between the lower part of the activation layer and the part except the lower part of the activation layer. JP '112's buffer layer 9 as seen in figure 1 is a flat structure without a step located as claimed in the present invention. On the other hand, in figure 24, the p buffer layers 9 do include n layers 28, but the buffer layers 9 are below an insulating film 10 and above the n base layer 1, and therefore, JP '112 does not disclose buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer as claimed.

Moreover, concerning claims 1, 7, 13 and 17, JP '112 fails to disclose, teach or suggest a step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer since no thickness measurements and comparison was made in the specification.

In addition since no thickness measurements were quantified, the concerning claims 3, 4, 5, 6, 11, 12, 15, 16, 20 of the present invention, JP '112 fails to disclose the range of thickness of the gate insulation layer, the polysilicon and the thickness of the step in the activation layer as claimed.

24. JP 04-096337 03/92 JAPAN (Kawasaki, JP'337)

JP'337 fails to disclose with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer as claimed in claims 1, 7, 13 and 17. JP'337 discloses a semiconductor device with a buffer layer 101 on a substrate 100 and below an active layer 102. The buffer layer 101 is below the active layer 102, however, as seen in Figs. 1 through 4, the buffer layer 101 does not have a step portion.

JP '337 fails to disclose a polycrytalline silicon layer as claimed in claims 17 and 7 and an amorphous silicon layer as claimed in claim 7. Looking at figure 4 of JP '337, a resist layer 103 is disclosed in addition to the active 102 and the buffer layers 101 on the substrate 100, but disclosure of the polycrystalline silicon or amorphous silicon layer.

25. JP 04-101432 04/92 JAPAN (Akiyama, JP'432)

JP'432, as seen in figure 1(e), discloses a substrate 101 with high density diffusion layers 110, oxide film 103 on and a gate electrode 104 formed on the oxide film. A polycrystalline silicon film 106 and the silicon oxide film107 is also disclosed with the silicon oxide film 107 shown in the interim product of figure 1(d). However, as seen both in figures 1(e) and 2(b), there is no disclose of the buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and therefore also the step of the buffer layer being

half or less of the thickness sum of the activation layer and the gate insulation layer is not disclosed according to claims 1, 7, 13 and 17.

26. JP 02-281634 11/90 JAPAN (Yamamoto, JP '634)

JP '634, as seen in figure 2(d), a drain region 2 is formed on the substrate and a p-type base region above the drain region, and a gate electrode 4 is formed through a polycrystalline layer. However, as seen both in figures 1(c) and 2(d), there is no disclose of the buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and therefore also the step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer is not disclosed according to claims 1, 7, 13 and 17.

27. JP 2002-329860 11/02 JAPAN (Lee, JP'860)

JP'860 discloses a conductive film 38a for a buffer being formed on opposite sides of the trench while being separated and a gate electrode 42a is formed in between through an insulation film. Looking at figure 3p of JP '860, the conductive film 38a for the buffer can be seen formed on opposite sides of the trench. However, as seen both in figures 3p, there is no disclose of the buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and therefore also the step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer is not disclosed according to claims 1, 7, 13 and 17.

28. JP 01-128575 05/89 JAPAN (Kawamura JP '575)

JP '575 discloses a silicon dioxide layer 6 formed in a polycrystalline silicon layer 3 and a gate insulating film 8 and gate electrode 9 are also formed as seen in figure 2. A single crystal silicon layer 7 is also flanked by the source and drain 10 and 11. However, as seen figure 2, there is no disclose of the buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and therefore also the step of the buffer layer being half or less of the thickness sum of the activation layer and the gate insulation layer is not disclosed according to claims 1, 7, 13 and 17.

29. KR 010082828 08/01 REPUBLIC OF KOREA (Kwon, KR'828)

Concerning claims 1, 13 and also claims 7 and 17, KR'828 fails to disclose step in the buffer being a half or less of the thickness sum of said activation layer and gate insulation layer and the buffer layer having the step formed between a lower part of said activation layer and a part except said lower part of said activation layer as claimed in claims 1, 7, 13 and 17. Looking at figure 11 of KR'828, a gate electrode 40 is formed in the transparent substrate 32 and a gate insulating layer

46 is on the substrate 32. A protective film 60 is formed around the source and drain electrodes 52 and 54 and a pixel electrode 68 is formed with the drain electrode and the protective film 60. Moreover, an active layer 48 is formed between the protective layer and the gate insulating layer. Therefore, as seen in figure 11 of KR '828, there is no buffer layer at the lower part of the activation layer 40 since the gate insulating layer 46 is at the lower part and the protective film 60 is on the active layer.

30. KR 100332124 03/02 REPUBLIC OF KOREA (EOM, KR'124)

Concerning claims 1, 7, 13 and 17, KR'124 fails to disclose the buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer and the step in the buffer being a half or less of the thickness sum of said activation layer and gate insulation layer and as claimed in claims 1, 7, 13 and 17.

As seen in figure 1 and 2 of KR'124, there is a silicon substrate 1 with a gate oxide layer 2A and a polysilicon layer 3 formed on the gate oxide layer 2A and a tungsten silicide layer 3 formed on the polysilicon layer 4. However, as seen in figures 1 and 2, there is no buffer layer having a step.

31. JP 2001-125135 05/01 JAPAN (Kawachi, JP'135)

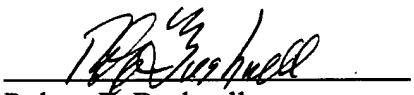
Concerning claims 1, 7, 13 and 17, JP'135 fails to disclose the buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer and the step in the buffer being a half or less of the thickness sum of said activation layer and gate insulation layer and as claimed in claims 1, 7, 13 and 17.

Six examples of thin film transistors are shown in JP'135 with one example in figures 3 and 1, shows a buffer layer 21 formed on substrate 1. An isolation insulator layer 24 is formed around polysilicon film 30 and below a gate electrode 10 and an interlayer insulation film 22 and a protective insulation layer 23 formed around the interlayer insulation film 22. An silicon dioxide film 20 is formed between the gate electrode and the isolation insulation layer. The interlayer insulation film 22 has a step, but the buffer layer 21 includes no step. Moreover, the flat buffer layer on paragraph 45 states that 300nm of buffer layer is deposited as shown on figure 18. Therefore, since no step is seen in the buffer layer 21 or any other buffer layer located on the lower side of the activation layer, then also JP'135 fails to disclose the buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer and the step in the buffer being a half or less of the thickness sum of said activation layer and gate insulation layer and as claimed in claims 1, 7, 13 and 17.

As shown above, the cited related art fail to disclose all of the claimed limitations as arranged in the claims under 35USC§102 and the above related art fail to teach or suggest all of the claimed limitations under 35USC§103. Moreover, even if the above references were combined in any

manner, they would still not make the present invention obvious since for example, none of the above references, as shown above, teach or suggest said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and said step being a half or less of the thickness sum of said activation layer and gate insulation layer as claimed in claims 1, 7, 13 and 17.

Respectfully Submitted



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Folio: P57012
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FEE TRANSMITTAL

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT	($) 130.00

Complete If Known	
Application Number	10/798,574
Filing Date	12 March 2004
First Named Inventor	HOON KIM
Examiner Name	FLYNN, NATHAN J.
Group/Art Unit	2826
Attorney Docket No.	P57012

METHOD OF PAYMENT (check one)

1. ■ The Commissioner is hereby authorized to charge ANY DEFICIENCY and credit ANY OVER PAYMENTS to:

Deposit Account Number: 02-4943
Deposit Account Number: _____

☐ Charge Any Additional Fee Required Under 37 C.F.R. §1.16 and 1.17.

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ■ **Payment Enclosed: (CHECK #48275)**

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	$
1002	350	2002	175	Design filing fee	$
1003	550	2003	275	Plant filing fee	$
1004	790	2004	395	Reissue filing fee	$
1005	160	2005	80	Provisional filing fee	$

SUBTOTAL (1) ($) .00

2. EXTRA CLAIM FEES

		Extra Claims	Fee from below	Fee Paid
Total claims	-20** =	x		=
Independent Claims	- 3** =	x		=
Multiple Dependent				=

** or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1201	88	2201	44	Independent claims in excess of 3
1202	18	2202	9	Claims in excess of 20
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) .00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge-late filing fee or oath	$
1052	50	2052	25	Surcharge-late provisional filing fee or cover sheet	$
1053	130	1053	130	Non-English specification	$
1812	2,520	1812	2,520	For filing a request for reexamination	$
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	$
1805	1,840 *	1805	1,840*	Requesting publication of SIR after Examiner action	$
1251	110	2251	55	Extension for reply within first month	$
1252	430	2252	215	Extension for reply within second month	$
1253	980	2253	490	Extension for reply within third month	$
1254	1,530	2254	765	Extension for reply within fourth month	$
1255	2,080	2255	1,040	Extension for reply within fifth month	$
1401	340	2401	170	Notice of Appeal	$
1402	340	2402	170	Filing a brief in support of an appeal	$
1403	300	2403	150	Request for oral hearing	$
1451	1,510	1451	1,510	Petition to institute a public use proceeding	$
1452	110	2452	55	Petition to revive - unavoidable	$
1453	1,370	2453	685	Petition to revive - unintentional	$
1501	1,370	2501	685	Utility issue fee (or reissue)	$
1502	490	2502	245	Design issue fee	$
1503	660	2503	330	Plant issue fee	$
1460	130	1460	130	Petitions to the Commissioner	$130.00
1807	50	1807	50	Processing fee for provisional applications	$
1806	180	1806	180	Submission of Information Disclosure Statement	$
8021	40	8021	40	Recording each patent assignment per property (Times number of properties)	$
1809	790	2809	395	Filing a submission after final rejection (37 C.F.R. §1.129(a))	$
1810	790	2810	395	For each additional invention to be examined (37 C.F.R. §1.129(b))	$
1801	790	2801	395	Request for Continued Examination (RCE)	$
Other Fee (specify) _____					$
Other Fee (specify) _____					$

** Reduced by Basic Filing Fee Paid

SUBTOTAL (3) $130.00

SUBMITTED BY

Typed or Printed Name	Robert E. Bushnell, Esq.	Reg. Number	27,774
Signature	/Robert E. Bushnell/	Date	1 November 2004
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